

EDS DL Mini Symposium

Invited Talk; EDS Distinguished Lecture

Challenges for Nanoelectronics: More Moore and More than Moore

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Abstract: Low power requirements by the International Technology Roadmap for Semiconductors (ITRS) dictate integration of high-k metal gates and novel devices such as FinFETs in CMOS technologies. To attend the current trend in device scaling for sub-14 nm CMOS technology (More Moore) EOT scaling of gate dielectric beyond 0.7 nm will be required. Various atomic layer deposition (ALD) methods of HfO₂-based high-k gate dielectrics are currently underway to enhance the dielectric constant and reliability in order to meet the above requirements. For example, cyclic deposition of ALD Hf_{1-x}Zr_xO₂ samples where the dielectrics were exposed to intermediate slot plane antenna (SPA) Ar plasma (DSDS) or annealing (DADA). In addition, variation of Al percentage and distribution in HfO₂ is carried out when HfAlO_x and HfO₂ are deposited by ALD in a layered structure. To further enhance the device performance, high mobility channel materials like Ge with high-k dielectrics are currently being integrated. Electrical performance in these devices depends on the high-k deposition process, precise selection of deposition parameters, predeposition surface treatments and subsequent annealing temperatures. Additionally, scaling limit is driving the incorporation of different Nano devices into Nano systems with functionalities that do not necessarily scale according to "Moore's Law", but provide additional value in different ways (More than Moore). This talk will outline some of the recent developments of EOT scaling of high-k gate dielectrics and some thin-film transistors that are key enablers of internet of things (IoT) sensor interfaces for flexible substrates (fabricating thin-film transistors using ALD zinc oxide as a substrate).

Speaker's Biography:

Prof. Durga Misra is a Professor in the Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, USA. His current research interests are in the areas of nanoelectronic/optoelectronic devices and circuits; especially in the area of nanometer CMOS gate stacks and device reliability. He is currently a Distinguished Lecturer of IEEE Electron Devices Society (EDS) and serving in the IEE EDS Board of Governors. He served as the EDS SRC Chair for North America East (Regions 1, 2, 3, and 7). He is a Fellow of the Electrochemical Society (ECS). He received the Thomas Collinan Award from the Dielectric Science & Technology Division of ECS. He is also the winner of the Electronic and Photonic Division Award from ECS. He edited and co-edited more than 40 books and conference proceedings in his field of research. He has published more than 100 technical articles in peer reviewed Journals and more than 160 articles in International Conference proceedings including 75 Invited Talks. He has graduated 17 PhD students and 35 MS students. He received the M.S. and Ph.D. degrees in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1985 and 1988, respectively.