EDS DL Mini Symposium

Keynote Talk; EDS Distinguished Lecture

Predictive Failure Analytics in VLSI

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Abstract:
As the technology pushes towards sub-22nm era, process, geometry, voltage and temperature (PVT) variability in devices can affect performance, functionality and power in circuits. This is where the need for predictive failure analytics is extremely critical. The failure issues related to logic and memory circuits are identified.

The talk describes how key statistical techniques and new algorithms can be effectively used to analyze and build robust circuits. The application of these algorithms for analysis of decoders to volatile to non-volatile memories are brought out. In addition how these methodologies are extended for "reliability prediction" and "hardware corroboration" is demonstrated. Also techniques to generate accurate parasitic capacitance modeling along with PVT-aware variability process variations for sub-22nm technologies and its incorporation into a physics-based statistical analysis methodology for accurate Vmin analysis are described. Finally the talk summarizes important issues in this field.

Speaker's Biography:

Dr. Rajiv V. Joshi is a research staff member and key technical lead at T. J. Watson research center, IBM. He received his B.Tech I.I.T (Bombay, India), M.S (M.I.T) and Dr. Eng. Sc. (Columbia University). His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5µm to 14nm. He has led successfully predictive failure analytic techniques for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He received 3 Outstanding Technical Achievement (OTAs), 3 highest Corporate Patent Portfolio awards for licensing contributions, holds 58 invention plateaus and has over 225 US patents and over 350 including international patents. He has authored and co-authored over 185 papers. He received the Best Editor Award from IEEE TVLSI journal. He is recipient of 2015 BMM award. He is inducted into New Jersey Inventor Hall of Fame in Aug 2014 along with pioneer Nikola Tesla. He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of IBM Academy of technology. He served as a Distinguished Lecturer for IEEE CAS and EDS society. He is IEEE, ISQED and World Technology Network fellow and distinguished alumnus of IIT Bombay. He is in the Board of Governors for IEEE CAS. He serves as an Associate Editor of TVLSI. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conference, ISQED and Advanced Metallization Program committees. He served as a general chair for IEEE ISLPED. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. Also he is in the industry liaison committee for IEEE CAS society.